

**TITLE**

**PROCESS OF DUAL DAMASCENE OR DAMASCENE**

**BACKGROUND OF THE INVENTION**

**Field of the Invention**

5       The present invention relates to a process of dual damascene or damascene, especially to a process with lowered cost and improved reliability.

**Description of the Related Art**

10       With the increase in integrity of integrated circuits, distances between the metal lines of semiconductor devices are becoming smaller. RC delay caused by the resistance between lines and the capacitance of the dielectric between the lines has become the main reason for delays in signal transmission and limits in device speed. Therefore, copper (Cu) lines and  
15       low k materials are continuously being improved for the fabrication of deep sub-micron devices to overcome the increase in parasitic resistance and capacitance caused by narrower line width in advanced process.

20       Dual damascene process replaces the current Al-Cu metal line process, a process of Back-End of Line (BEOL) of the wafer manufacturing, used after forming the contact plug on the silicon substrate and possibly repeated several times based on the designed number of metal line layers of the device.

25       Traditional dual damascene process flow can be all-in-one chamber, all-in-one system, or others. As shown in Fig.1a, all-in-one chamber type uses an all-in-one chamber machine comprising loadlocks 111, mainframe 113, and process chamber

112. Like US 2003/0032278 "All dual damascene oxide etch process steps on one confined plasma chamber", the all-in-one chamber type accomplishes all dual damascene steps in one chamber. The all-in-one chamber using etching apparatus for ashing has a high Rc failure risk, difficulty in application to low K materials, and low reliability. As shown in Fig.1b, an all-in-one system type uses an all-in-one system machine comprising loadlocks 121, mainframe 124, process chamber 122, and process chamber 123. When an all-in-one system type uses etching apparatus for ashing the cost of the process is high, and the process synchronization is poor.

#### **SUMMARY OF THE INVENTION**

For this reason, there is a need for a dual damascene process providing good reliability and lower cost.

To achieve this aim, the present invention provides a dual damascene process comprising via/trench etching module, dry cleaning module (DCM), and wet cleaning module. The DCM can include resist ashing, contact ashing, stop layer removal, metal line cleaning, and dielectric layer repair. In the present invention, the via/trench etching and dry cleaning modules are performed in different chambers of different machines. The present invention comprises a via forming and trench forming processes with segments thereof respectively falling into each of the 3 process modules. The via forming process comprises providing an etching apparatus, a DCM machine and a wafer, the wafer having a metal line, a stop layer, a dielectric layer, and a photoresist layer, etching the dielectric layer in the etching apparatus to form a via hole, ashing the photoresist

in the DCM machine, and wet cleaning the wafer. The trench forming process comprises providing an etching apparatus, a DCM machine, and a wafer, the wafer having a metal line, a stop layer, a dielectric layer, a contact, and a photoresist layer, etching  
5 the dielectric layer and the contact in the etching apparatus to form a trench, ashing the photoresist and the contact in the DCM machine, and wet cleaning the wafer.

The present invention has the advantages of good production capability, lower costs and defects, and extendibility to many  
10 low K materials.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

Fig. 1a shows a conventional all-in-one chamber machine;

Fig. 1b shows a conventional all-in-one system machine;

Fig. 2 shows an etching apparatus and a DCM machine of the  
15 present invention;

Figs. 3a to 3f are sectional views showing a dual damascene process according to the present invention.

#### **DETAILED DESCRIPTION OF THE INVENTION**

In terms of a process flow, the present invention comprises  
20 via/trench etching module, dry cleaning module (DCM), and wet cleaning module. As shown in Fig.2, the via/trench etching and dry cleaning modules of the present invention are performed in different chambers of different machines. The etching apparatus 210 comprises loadlocks 211, mainframe 213 and process  
25 chamber 212. After etching, a wafer is moved to a DCM machine. The DCM machine 220 comprises loadlocks 221, mainframe 223 and process chamber 222. The method of the present invention

improves the synchronization problem present in conventional all-in-one systems.

The present invention comprises a via forming and trench forming processes with segments thereof respectively falling into each of the 3 process modules. Figs. 3a-3c illustrate the via forming process. In Fig. 3a, a wafer 300 having a metal line 310, a stop layer 311, a dielectric layer 312, and a photoresist layer 313 for defining a via pattern is provided. The wafer is placed in a process chamber of an etching apparatus. As shown in Fig. 3b, in the process chamber of the etching apparatus, the dielectric layer 312 of the wafer 300 is etched to form a via hole 320. After etching, the wafer 300 is moved to a DCM machine. As shown in Fig. 3c, in a process chamber of the DCM machine, the photoresist 313 is stripped by ashing. After processing in the DCM machine, the wafer 300 is moved to a wet cleaning machine to be cleaned. The wet cleaning step can use DHF or DI water as a cleaning solvent.

The metal line can be made of copper.

The dielectric layer can comprise low k materials.

In the ashing step, a reaction gas contained in the processing chamber comprises  $O_2$ ,  $H_2O$ ,  $H_2$ ,  $NH_3$  with or without  $N_2$ , He, or Ar. The processing chamber of the DCM machine ashes with an inductively coupled plasma generated by a dual-power (source power plus bias power) tool.

After the via forming process, the wafer is sent to plug a contact and undergoes a trench lithography process.

After the trench lithography process, the wafer is moved to the etching apparatus for trench forming. Figs. 3d-3f illustrate the trench forming process. In Fig. 3d, a wafer 300

having a metal line 310, a stop layer 311, a dielectric layer 312, a contact 314, and a photoresist layer 315 is provided. The wafer is placed in the process chamber of the etching apparatus. As shown in Fig. 3e, in the process chamber of the etching apparatus, the dielectric layer 312 and the contact 314 of the wafer 300 are etched to form a trench 330. After etching, the wafer 300 is moved to a DCM machine. As shown in Fig. 3f, in the process chamber of the DCM machine, the photoresist 315 and the contact 314 is stripped by ashing, and the stop layer 311 is also removed by ashing. As well, in the process chamber of the DCM machine, the metal line 310 can be cleaned and the dielectric layer 312 can be repaired by CVD (Chemical Vapor Deposition). After processing in the DCM machine, the wafer 300 is moved to the wet cleaning machine to be cleaned. The wet cleaning step can use DHF or DI water as a cleaning solvent.

As mentioned above, in the ashing step, a reaction gas contained in the processing chamber comprises  $O_2$ ,  $H_2O$ ,  $H_2$ ,  $NH_3$  with or without  $N_2$ , He, or Ar.

The stop layer removing step can use  $CxFy$ ,  $CxFyHz$ ,  $SF_6$ , or  $NF_3$  as removal chemistry, with or without inert gas.

In the metal line cleaning step, the dry cleaning chemistry can be  $O_2$  or  $H_2$ , with or without inert gas. The reaction temperature of the metal line cleaning step is between  $-10^\circ C$  to  $300^\circ C$ .

In the dielectric layer repair step, the repair chemistry can be  $H_2$  or halogen-silane.

The present invention improves the synchronization problems prevalent in conventional all-in-one systems. By replacing etching apparatus with specially designed DCM machine

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as a means of ashing, the present invention provides better electrical results and decreases the cost. Because etching and ashing are performed in different chambers, the particle condition in the process chamber is also improved, as is  
5 reliability of the product. As well, the present invention can be applied to dual damascene structures having any kind of low k material therein.

As well, the process of the present invention can be also applied in damascene process to achieve the advantages mentioned  
10 above.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications  
15 and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.